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**PATENT APPLICATION**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Isao YOKOKAWA et al.

Group Art Unit: 2818

Application No.: 10/782,838

Examiner: C. LUU

Filed: February 23, 2004

Docket No.: 118749

For: METHOD FOR PRODUCING SOI WAFER AND SOI WAFER

**REQUEST FOR RECONSIDERATION**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

In reply to the June 13, 2005 Office Action, reconsideration of the rejection is respectfully requested in light of the following remarks. Claims 1-8 are pending in this application.

The Office Action rejects claims 1-8 under 35 U.S.C. §103(a) over Aga et al. (U.S. Patent No. 6,140,210) in view of Yamagata (U.S. Patent No. 6,653,209). The rejection is respectfully traversed.

In particular, none of the applied references, alone or in combination, disclose or suggest a method of producing an SOI wafer in which an SOI layer is formed on a buried oxide film wherein, assuming that X represents the thickness of the buried oxide film and Y represents the thickness of the SOI layer in the SOI wafer immediately after delaminating at the ion-implanted layer, the thickness X of the buried oxide film is  $X \leq 100$ , and the ion implantation is carried out with the ion implantation conditions being set such that the sum  $X + Y$  satisfies  $X + Y > 1500 - 14X$ , as recited in independent claim 1.

Specifically, Aga teaches a method of fabricating an SOI wafer wherein an oxide film is formed on the surface of at least one of two silicon wafers, hydrogen ions or rare gas ions are implanted into the upper surface of one of the two silicon wafers, and a heat treatment is performed in order to delaminate the portion of the ion-implanted wafer (Abstract). Also, the purpose of Aga is to create a uniform film thickness of the SOI layer (Col. 3, lines 44-51). Moreover, Aga teaches SOI wafers in which the SOI layer has a thickness of 870 nm and the buried oxide layer has a thickness of 400 nm (Col. 6, lines 10-15). However, with such large thicknesses for the buried oxide layer, the problem of blisters and voids is not crucial, as this problem is crucial only for a buried oxide film with a thickness that is 100 nm or smaller. Moreover, because the thickness of the buried oxide layer is so large, the expression  $1500 - 14X$ , wherein  $X$  is the thickness of the buried oxide layer, is meaningless because  $1500 - 14X$  would result in a negative number. Accordingly, Aga does not teach or suggest that immediately after delaminating at the ion-implanted layer, when the thickness  $X$  of the buried oxide film is smaller than or equal to 100, the ion implantation is carried out such that  $X + Y > 1500 - 14X$ , as recited in independent claim 1.

Yamagata does not make up for this deficiency. Yamagata teaches a silicon ultra thin film SOI layer to decrease the thickness of a silicon thin film without deterioration of the quality of the film while avoiding the surface roughness due to speed increasing oxidation of crystal defect portions (Abstract). Specifically, Yamagata teaches a step of wet-cleaning the silicon thin film on the insulating surface to decrease the thickness of the silicon thin film to 100 nm or smaller (Col. 3, lines 28-36). The Office Action indicates that Yamagata teaches a thickness of a buried oxide film  $X \leq 100$  nm and points to Col. 6, lines 62-65 of Yamagata. However, the indicated portion of Yamagata teaches hydrogen annealing in order to smooth the surface for an hour in order to obtain an SOI wafer that includes a 100 nm silicon layer and a 100 nm buried silicon oxide layer. Accordingly, although Yamagata may indicate a

buried oxide layer of 100 nm, Yamagata does not teach that the thickness of the SOI layer immediately after delaminating at the ion-implanted layer, when the thickness X of the buried oxide film is  $\leq 100$ , the condition  $X + Y$  is  $> 1500 - 14X$ , as recited in independent claim 1. Specifically, the thicknesses indicated in Yamagata are achieved after separating the wafer at the porous layer, not immediately after delaminating, as recited in independent claim 1.

As discussed above, Aga teaches an SOI wafer with an oxide film that has a thickness of about 400 nm. Yamagata's First Example teaches a fabrication process of an SOI wafer in which a porous layer is formed on a device wafer by anodization (First Example, col. 5, line 46 - col. 7, line 16). In Yamagata's First Example, no ion implantation is used and therefore it would not have been obvious to replace Yamagata's anodization method with Aga's ion implantation delamination method. Accordingly, Yamagata and Aga cannot be combined to arrive at the claimed invention.

Moreover, although Yamagata's Fifth Example teaches ion implantation, the film thickness achieved is in the range of 400 nm (Col. 12, line 1). As such, a combination of Aga and Yamagata's Fifth Example would result in an SOI wafer with a buried oxide film thickness of 400 nm obtained via ion implantation delamination, and as such would not render obvious the features recited in independent claim 1.

Moreover, because a combination of the applied art does not disclose the features of claim 1, it cannot provide the advantages of the claimed invention. Aga does not suggest any motivation for the fabrication of an SOI wafer with a buried oxide layer thickness that is smaller than or equal to 100 nm. No disclosure has been cited to provide the motivation for modifying Aga to provide the advantages of the claimed invention. Thus, such modification constitutes an impermissible use of Applicants' disclosure based on hindsight reasoning.

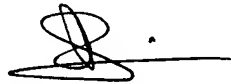
Thus, a combination of the applied references would not arrive at the claimed invention and it would not have been obvious to combine Aga and Yamagata to disclose or

suggest the subject matter of independent claim 1. As such, independent claim 1 and its dependent claims are patentable over a combination of the applied references. Thus, withdrawal of the rejection of the claims under 35 U.S.C. §103(a) is respectfully requested.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-8 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



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